UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,045	07/15/2003	Rajarshi Bhattacharya	1-4-2-2-1	7529

7590 11/03/2009

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
OCHOA, JUAN CARLOS	
ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
11/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,045	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	JUAN C. OCHOA	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/17/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6 and 8-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6 and 8-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to BPAI Decision - Examiner Affirmed Decision of 06/15/2009 and arguments filed 08/17/2009.

2. Examiner Mary C. Jacob is no longer prosecuting this application. Examiner Juan Carlos Ochoa is taking over the prosecution of this application.

3. Claims 1, 3, 4, 6, and 8–23 are presented for examination.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 08/17/2009 has been entered.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 3, 4, 6, and 8–23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boggio et al., (Boggio hereinafter), "NetworkDesigner–Artifex–OptSim: A Suite of Integrated Software Tools for Synthesis and Analysis of High Speed Networks", (see PTO-892 Notice of Reference Cited dated 06/19/2006), in view of Sun et al., (Sun hereinafter), "Simulation Studies of Multiplexing and Demultiplexing Performance in ATM Switch Fabrics", (see PTO-892 Notice of Reference Cited dated 06/19/2006), and further in view of Ishida et al., (Ishida hereinafter), "A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System", (see PTO-892 Notice of Reference Cited dated 06/19/2006).

9. As to Claims 1, 16, 18 and 19, Boggio teaches: a method of simulating the operation of an optical network and corresponding switching scheme (page 29, section 2, paragraph 4; page 30, column 1, paragraph 1, lines 11-15) comprising a plurality of integrated circuits (page 28, column 2, bullet 3; page 29, column 1, paragraph 5, sentence 3; page 30, column 2, lines 6-9), utilizing a software-based development tool, the method comprising the steps of: providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the optical network (page 28, column 2, 4th and 5th bullets; page 29, section 2, paragraph 3); automatically generating a simulation configuration for the optical network based on current values of the configurable parameters, the simulation configuration being generated without requiring further user input, the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters (page 30, column 1, lines 7-15). As to the storage, memory and processing device, since Boggio is directed to software tools running simulations including a debugger, report generator (page 30, column 1, lines 44-46), libraries (Figure 1, "Equipment Library") and displaying output on a graphical user interface (Figure 12), it is understood that the software development tool must run on a computer system containing memory, processing device and a storage device; wherein the one or more configurable parameters of the switch fabric comprise one or more configurable parameters of each of the integrated circuits and one or more configurable parameters of a base device specified for the designated chip set (page 30, column 1, lines 1-7; page 10, column 2, lines 6-9);

10. As to Claim 6, Boggio teaches: wherein the interface includes a listing of the integrated circuits (page 29, column 1, paragraph 5, sentence 3; page 30, column 1, lines 1-7).

11. As to Claim 12, Boggio teaches: wherein the software-based development tool comprises an automatic configuration generation module which generates the simulation configuration for the optical network based on the current values of the configurable parameters (page 30, column 1, lines 7-15).

12. As to Claim 13, Boggio teaches: wherein the simulation configuration is generated utilizing an object-oriented programming construct comprising a base class, corresponding to a base device specified for the plurality of integrated circuits, and an associated generation interface (page 30, column 1, lines 37-40; page 32, column 2, lines 27-35).

13. As to Claim 14, Boggio teaches: wherein the generation interface declares a generate function that is implemented by each of a plurality of generators, each of the plurality of generators corresponding to a different configuration of the optical network (page 30, column 1, lines 7-15).

14. As to Claim 17, Boggio teaches: wherein the software-based development tool comprises a simulator control module (page 30, column 2, lines 3-5, 14-15), a set of interfaces (Figure 3; Figure 5; Figure 11), and circuit element modules each corresponding to an associated one of the integrated circuits (column 30, lines 6-9).

15. Boggio does not expressly teach (claims 1, 18, 19) simulating the operation of at least one switch fabric and wherein each integrated circuit of the designated chip set

corresponds to a specified ingress device, a specified cross-connect device or a specified egress device; and wherein the one or more configurable parameters of a given integrated circuit are determined by the correspondence of the given integrated circuit to the specified device; (claim 3) wherein the at least one switch fabric comprises at least one multistage switch fabric; (claim 4) wherein the circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices; (claims 8, 9, 10, 11) wherein the configurable parameters comprise a number of ports of the electronic system, switching capacity, configuration type, such as one of a centralized configuration, stackable configuration or distributed configuration; (claim 12) automatically generating the simulation configuration for the switch fabric based on the current values of configurable parameters; (claim 14) the plurality of generators corresponding to a different configuration of the switch fabric; (claim 15) the configuration types consisting of centralized configuration, stackable configuration or distributed configurations of the switch fabric; (claim 20) the interface permits user selection of each of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric; (claim 21) wherein the one or more configurable parameters of the switch fabric comprise a clock speed of at least a given one of the integrated circuits and a clock speed of the base device specified for the designated chip set; (claim 22) the switching capacity of the switch fabric determines a number of integrated circuits included in the switch fabric; and (claim 23) wherein each integrated circuit has at least one block function associated therewith (Figure 2 and description).

16. Sun teaches (claims 1, 18, 19) a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality (Abstract) and wherein each integrated circuit of the designated chip set corresponds to a specified ingress device, a specified cross-connect device or a specified egress device; and wherein the one or more configurable parameters of a given integrated circuit are determined by the correspondence of the given integrated circuit to the specified device (Figure 2 and description), (claim 3) wherein the at least one switch fabric comprises a multistage switch fabric, (claim 4) the integrated circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices (Figure 2 and description), (claim 11) wherein the configurable parameters comprise a number of ports of the electronic system (Abstract, sentence 2; page 21/1, paragraph 6, sentence 4 and 5; page 21/2, paragraph 3), (claim 8) and switching capacity (Abstract, sentence 2; Figure 2; page 21/2, 3rd paragraph), (claim 9) a configuration type, (claim 10) use of a centralized configuration for a multistage switch fabric of the electronic system, (claims 14, 15) the ability to build other configurations (Figure 2, page 21/3, paragraph 1); (claim 12) generating a simulation configuration for the switch fabric based on the current values of configurable parameters (pages 21/2-21/3 "Modelling Switching Fabrics"); (claim 20) the interface permits user selection of each of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric (page 21/3, 5th paragraph); (claim 21) wherein the one or more configurable parameters of the switch fabric comprise a clock speed of at least a given

one of the integrated circuits and a clock speed of the base device specified for the designated chip set (page 21/3, 3rd & 4th paragraphs); (claim 22) the switching capacity of the switch fabric determines a number of integrated circuits included in the switch fabric (pages 21/2-21/3 "Modelling Switching Fabrics"); and (claim 23) wherein each integrated circuit has at least one block function associated therewith (Figure 2 and description).

17. Boggio and Sun are analogous art since they are both directed to the modeling and simulation of a network.

18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software development tool for an optical network as disclosed in Boggio to include the modeling of a multistage switch fabric wherein the at least one switch fabric comprises a multistage switch fabric, the integrated circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices, wherein the configurable parameters comprise a number of ports of the electronic system, switching capacity, a configuration type, the use of a centralized configuration for a multistage switch fabric of the electronic system, the ability to build other configurations and generating a simulation configuration for the switch fabric based on the current values of configurable parameters as taught in Sun since Sun teaches a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality (Abstract).

19. Boggio in view of Sun teach a software development tool for the automatic generation of a simulation configuration of a switch fabric including the specification between integrated circuits that satisfy configurable parameters.

20. Boggio in view of Sun do not expressly teach integrated circuits of a designated chip set.

21. Ishida teaches an ultra high speed 8-b multiplexer and demultiplexer chip set that has been developed for the synchronous optical network (SONET) as a key component of next-generation optical fiber communication systems that will require higher data bit rates for future increases in transmission capacity (page 1936, column 1).

22. Boggio in view of Sun and Ishida are analogous art since they are directed to the design of a communication network.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the design of the at least one switch fabric including user configurable parameters of integrated circuits as taught by Boggio to include a chip set as taught in Ishida since Ishida teaches a high speed multiplexer and demultiplexer chip set that is a key component of a next-generation optical fiber communications systems that will require higher data bit rates for future increases in transmission capacity (page 1936, column 1).

Response to Arguments

24. Regarding the arguments with respect to the rejection under 102 and 103, those rejections are rendered moot by the amendment.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUAN C. OCHOA whose telephone number is (571)272-2625. The examiner can normally be reached on 7:30AM - 4:00 PM.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. C. O./ 11/3/2009
Examiner, Art Unit 2123

/Paul L Rodriguez/
Supervisory Patent Examiner, Art Unit 2123